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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,702	02/07/2001	Anilkumar C. Bhatt	END919960141US2	5311

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EXAMINER
ALCALA, JOSE H

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/778,702	BHATT ET AL.
	Examiner	Art Unit
	Jose H Alcala	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-20 and 22-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-20 and 22-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 1/27/03 have been dissaproved. The drawings are still improperly crosshatched. It is pointed out that the crosshatching pattern of the dielectric substrate and the filler material inside the through hole, should be the same pattern (the pattern used in this amendment for the filler material), since both are dielectric materials. 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 9 ,22 and 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reed (US Patent No. 4,964,948).

4. Reed teaches a printed wiring board (device of figure 12) comprising: (a) a dielectric substrate (reference number 20) having upper and lower surfaces; (b) at least one landless filled plated through hole (reference number 38) disposed through the substrate from the upper to the lower surface, the through hole having a first diameter,(c) the through hole further comprising an inner surface extending from the upper to the lower surface, the inner surface plated with a conductive metal plating (reference number 36) , the inner surface plating having an upper end aligned with the substrate upper surface and a lower end aligned with the substrate lower surface; (d)the through hole filled with a filler composition (reference number 44) having upper and lower surfaces, wherein the filler composition upper surface is aligned with the dielectric substrate upper surface and the through hole inner surface plating upper end, the filler composition upper surface, substrate upper surface and inner surface plating upper end thereby defining a smooth upper subcomposite surface; and (e) a first circuitry (Reference number 46) additively plated onto said upper subcomposite surface and electrically connected to said plated through hole, said first circuitry further comprising circuit lines (column 9, lines 3-5), but fails to explicitly teach that the line width is approximately equal or less than the first diameter.

It is well known in the art to make circuit lines having the smallest width possible, in order to improve integration of an electronic device or printed wiring board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reed in order to reduce the line width to be approximately equal or less than the first diameter, in order to improve integration. In addition, it has

been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claims 22, Reeds teaches that the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates (column 4, lines 27-35).

Regarding Claim 25, Reeds teaches that the inner surface conductive metal plating has a thickness, and suggests to reduce the thickness (column 7, lines 28-37) , in order to reduce the size of the hole in a controlled manner to maintain the size close to that originally drilled, but fails to explicitly teach that the thickness is from about 0.1 mils to about 4.0.mils. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reed in order to reduce the thickness is from about 0.1 mils to about 4.0.mils, in order to in order to reduce the size of the hole in a controlled manner to maintain the size close to that originally drilled. In addition, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

5. Claims 10-14,23,24,26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed (US Patent No. 4,964,948) in view of Reimann (US Patent No. 4,663,497).

Regarding Claim 10, Reed teaches all of the elements of the instant claimed invention as modified supra for claim 9, but fails to explicitly teach that the first circuitry further has an aspect ratio greater than about 0.5. Reimann teaches in figure 13, that

the circuitry lines (reference number 54) have an aspect ratio greater than about 0.5. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Reed and Reimann in order to have the first circuitry having an aspect ratio greater than about 0.5, thus preventing undesired etching of the feed-through vias even in the event of misregistration of the photoresist material.

Regarding Claim 11, Reed teaches all of the elements of the instant claimed invention as modified supra for claim 9, but fails to explicitly teach that the first circuitry further has an aspect ratio greater than about 1. Reimann teaches in figure 13, that the circuitry lines (reference number 54) have an aspect ratio greater than about 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Reed and Reimann in order to have the first circuitry having an aspect ratio greater than about 1, thus preventing undesired etching of the feed-through vias even in the event of misregistration of the photoresist material.

Regarding Claims 12-14, Reed fails to explicitly teach that said first circuitry further comprises an upper conductive metal pad plated onto the through hole inner surface plating upper end and the fill composition upper surface, the pad having a second diameter about equal to the first diameter. Reimann teaches that said first circuitry further comprises an upper conductive metal pad (reference number 40) plated onto the through hole and the fill composition upper surface, the pad having a second diameter about equal to the first diameter. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Reed and Reimann in order to have an upper conductive metal pad plated onto the through hole

inner surface plating upper end and the fill composition upper surface, the pad having a second diameter about equal to the first diameter, thus preventing undesired etching of the feed-through vias even in the event of misregistration of the photoresist material and preventing the filler material to get out of the through hole.

Regarding Claims 23 and 24, Reeds teaches that the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates (column 4, lines 27-35).

Regarding Claims 26 and 27, Reeds teaches that the inner surface conductive metal plating has a thickness, and suggests to reduce the thickness (column 7, lines 28-37), in order to reduce the size of the hole in a controlled manner to maintain the size close to that originally drilled, but fails to explicitly teach that the thickness is from about 0.1 mils to about 4.0.mils. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reed in order to reduce the thickness is from about 0.1 mils to about 4.0.mils, in order to in order to reduce the size of the hole in a controlled manner to maintain the size close to that originally drilled. In addition, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

6. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed (US Patent No. 4,964,948) in view of Reimann (US Patent No. 4,663,497), and further in view of Kumagai et al. (US Patent No. 4,942,079).

Regarding claims 15-17, Reeds as modified by Reimann teaches all the elements of the instant claimed invention as stated supra for claims 9-11, but fails to further teach a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry on said dielectric substrate, said layer of dielectric material having at least one via formed therein. Kumagai teaches a layer of dielectric material (reference number 92)disposed on a dielectric substrate (reference number 71) and overlying a first circuitry (reference number 81) on said dielectric substrate, said layer of dielectric material having at least one via (reference number 91) formed therein.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the combination of Reed and Reimann, with the teachings of Kumagai, in order to have a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry on said dielectric substrate, said layer of dielectric material having at least one via formed therein, thus making the board capable of having a plurality of electronic part constituent units built in sufficiently separated from each other, but improving integration at the same time.

Regarding claims 18-20, Reeds as modified by Reimann, fails to further teach a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry through the at least one via. Kumagai teaches a second circuitry (reference number 93) disposed on a top surface of said layer of dielectric material (reference number 92) and electrically connected to the first circuitry (reference number 81) through the at least one via (reference number 91).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the combination of Reed and Reimann, with the teachings of Kumagai, in order to have a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry through the at least one via, thus making the board capable of having a plurality of electronic part constituent units built in sufficiently separated from each other, but improving integration at the same.

Response to Arguments

Applicant's arguments with respect to claims 9-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have some of the elements of the instant claimed invention: Bross et al. (US Patent No. 5,517,751), Shibuya et al. (US Patent No. 5,576,518) and Chakravorty et al. (US Patent No. 5,436,504). Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

9. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
February 10, 2003

David A. Zarneke
AV2827